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(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER
108574

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (if known, sec 37 C.F.R.1.5)
09/806934

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/06091	November 1, 1999	December 2, 1998

TITLE OF INVENTION
PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

APPLICANT FOR DO/EO/US
Masayuki KIKUSHIMA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☒ Other items or information: Request for Approval of Drawing Corrections

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/806934	INTERNATIONAL APPLICATION NO. PCT/JP99/06091	ATTORNEY'S DOCKET NUMBER 108574

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO ....$860.00 International preliminary examination fee paid to USPTO (57 CFR1.482) ....$690.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ....$710.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ....$1,000.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	32 - 20 =	12	X $ 18.00	$216.00	
Independent Claims	5 - 3 =	2	X $ 80.00	$160.00	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1,236.00	
Reduction by 1/2 for filing by small entity, if applicable.			-	$	
SUBTOTAL =				$1,236.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)).			+	$	
TOTAL NATIONAL FEE =				$1,236.00	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 117886 in the amount of $1,236.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
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NAME: James A. Oliff
REGISTRATION NUMBER: 27,075

NAME: Eric D. Morehouse
REGISTRATION NUMBER: 38,565

(1390 Rev.10-00)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masayuki KIKUSHIMA

Application No.: U.S. National Stage of PCT/JP99/06091

Filed: April 6, 2001 Docket No.: 108574

For: PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE ABSTRACT:

Please replace the Abstract with the Substitute Abstract attached hereto.

IN THE SPECIFICATION:

Page 1, lines 1-4, delete current paragraph and insert therefor:

PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

Page 1, line 8, delete current paragraph and insert therefor:

2. Description of Related Art

Page 2, after paragraph **[0005]**, insert new paragraph heading as follows:

SUMMARY OF THE INVENTION

Please delete page 2, line 22.

Please replace paragraph **[0008]** as follows:

[0008] One exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element both included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern on the base through a plurality of bumps.

Please replace paragraph **[0009]** as follows:

[0009] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on the center portion of an active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0010]** as follows:

[0010] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about the center of an active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0011]** as follows:

[0011] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0012]** as follows:

[0012] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

Please replace paragraph **[0013]** as follows:

[0013] In another exemplary embodiment of the present invention, the piezoelectric device described above further includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator, the layered part including at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

Please replace paragraph **[0014]** as follows:

[0014] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0015]** as follows:

[0015] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base may consist of a ceramic composite substrate.

Please replace paragraph **[0016]** as follows:

[0016] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

Please replace paragraph **[0017]** as follows:

[0017] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

Please replace paragraph **[0018]** as follows:

[0018] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the protrusion is formed in each of the side walls of the base facing the two sides along the longitudinal direction of the semiconductor integrated circuit.

Please replace paragraph **[0019]** as follows:

[0019] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the protrusion formed in the side wall of the base has substantially the same height as, or is higher than, the semiconductor integrated circuit.

Please replace paragraph **[0020]** as follows:

[0020] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

Please replace paragraph **[0021]** as follows:

[0021] Another exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated

circuit is mounted in the opening, and the semiconductor integrated circuit is connected to the electrode pattern of the base through the plurality of bumps.

Please replace paragraph **[0022]** as follows:

[0022] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals at the center portion of the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0023]** as follows:

[0023] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0024]** as follows:

[0024] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

Please replace paragraph **[0025]** as follows:

[0025] In another exemplary embodiment of the present invention, the piezoelectric device described above, further includes a layered part on which the piezoelectric resonator is mounted and which surrounds the semiconductor integrated circuit, the layered part including at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

Please replace paragraph **[0026]** as follows:

[0026] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the

semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0027]** as follows:

[0027] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base includes a ceramic composite substrate.

Please replace paragraph **[0028]** as follows:

[0028] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

Please replace paragraph **[0029]** as follows:

[0029] Another exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern is formed, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern through the plurality of bumps by ultrasonic bonding.

Please replace paragraph **[0030]** as follows:

[0030] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to the two opposing sides of the active

element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

Please replace paragraph **[0031]** as follows:

[0031] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

Please replace paragraph **[0032]** as follows:

[0032] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0033]** as follows:

[0033] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

Please replace paragraph **[0034]** as follows:

[0034] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base consists of a ceramic composite substrate.

Please replace paragraph **[0035]** as follows:

[0035] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

Please replace paragraph **[0036]** as follows:

[0036] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

Please replace paragraph **[0037]** as follows:

[0037] In another exemplary embodiment of the present invention, the piezoelectric device described above includes the semiconductor integrated circuit and the piezoelectric resonator element in included in the package, wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

Please replace paragraph **[0038]** as follows:

[0038] Another exemplary embodiment of the present invention is a method for manufacturing a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated

circuit during the ultrasonic bonding; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Please replace paragraph **[0039]** as follows:

[0039] Another exemplary embodiment of the present invention is a method for manufacturing a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step; a step of filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Page 7, line 22, delete current paragraph and insert therefor:

BRIEF DESCRIPTION OF THE DRAWINGS

Please replace paragraph **[0040]** as follows:

[0040] Figs. 1(A)-(B) are structural diagrams of a piezoelectric device according to the present invention;

Fig. 2 is a diagram illustrating the formation of a bump on a wafer of the piezoelectric device of the present invention;

Fig. 3 is a diagram showing the shape of the bump of the piezoelectric device of the present invention;

Fig. 4 is a diagram showing the shape of another bump of the piezoelectric device of the present invention;

Fig. 5 is a process diagram illustrating a flip-chip bonding process of the present invention;

Fig. 6 is a stress distribution map according to FEM analysis;

Fig. 7 is a structural diagram showing another embodiment of the present invention;

Fig. 8 is a structural diagram showing another embodiment of the present invention;

Fig. 9 is a structural diagram showing another embodiment of the present invention;

Figs. 10(A)-(B) are a plan view and a front view, respectively, showing another embodiment of the present invention;

Figs. 11(A)-(B) are a plan view and a front view, respectively, showing another embodiment of the present invention;

Fig. 12 is a structural diagram showing another embodiment of the present invention;

Fig. 13 is a structural diagram showing a cross-section of a bonded portion of the present invention;

Fig. 14 is a structural diagram showing yet another embodiment of the quartz crystal oscillator of the present invention;

Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14; and

Figs. 16(A)-(B) are structural diagrams of a conventional piezoelectric device.

Page 8, line 25, delete current paragraph and insert therefor:

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Please replace paragraph **[0043]** as follows:

[0043] Figs. 1(A)-(B) are structural diagrams of a surface-mount type quartz crystal oscillator according to an embodiment of the present invention.

Please replace paragraph **[0044]** as follows:

[0044] As shown in a plan view of Fig. 1(A) and in a front view of Fig. 1(B), on a first layer of a base 1 consisting of a ceramic insulating substrate having at least three layers and a seal ring of Fe-Ni alloy or the like, stamped to a frame shape, an electrode pattern 3 for forming a connection with a semiconductor integrated circuit (IC chip: hereinafter referred to as the IC chip) 2 is metallized by means of printing by using metal wiring material such as W (tungsten), Mo (molybdenum). On the top thereof, Ni plating and Au plating, etc., are provided.

Please replace paragraph **[0058]** as follows:

[0058] The wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal collet, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned and is chip-mounted on a mounting area of the base 1 with high precision by a system such as an image recognition system provided in the flip-chip bonding apparatus.

Please replace paragraph **[0066]** as follows:

[0066] As shown in Figs. 1(A)-(B), a configuration in which an opening 16 is formed in the center of the base 1 and the IC chip 2 is mounted in the center of the opening 16 is employed. Thus, when the quartz crystal oscillator 13 is exposed to stress, by this configuration, the stress is evenly applied to the IC chip 2, preventing the stress from concentrating in a specific portion.

Please replace paragraph **[0077]** as follows:

[0077] As shown in Figs. 1(A)-(B), the AT-cut quartz crystal resonator 6 is connected and fixed by the conductive adhesive 9 to mounting electrodes 21 and 22 of the mounting portion 8 provided in the second layer 5 of the base 1.

Please replace paragraph **[0089]** as follows:

[0089] Furthermore, in order for the underfill material 23 to properly permeate to the bonded portion of the bumps 4, the second layer 5 on which the AT-cut quartz crystal resonator 6 is mounted may include two layers, i.e., a first layer 24 and a second layer 25. The opening portion of the first layer 24 is formed to be larger than the opening portion of the second layer 25. By forming the second layer 25 in such a manner, the underfill material 23 properly permeates to the bonded portion of the bumps 4 and a highly reliable bonding structure is obtained.

Please replace paragraph **[0107]** as follows:

[0107] In this embodiment, the vibration direction US2 of the ultrasonic waves for ultrasonic bonding and for forming bumps on the IC chip 2 shown in Fig. 15, and vibration direction US1 of the ultrasonic waves for performing a ultrasonic bonding of the IC chip 2 and the base 1 shown in Fig. 14 are set to be different, preferably, in directions which differ from one another by 90 degrees.

IN THE CLAIMS:

Please replace claims 1-5, 7-17 and 19-30 as follows:

1. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern on the base through the plurality of bumps.

2. (Amended) The piezoelectric device according to claim 1, the plurality of bumps formed on the semiconductor integrated circuit being formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. (Amended) The piezoelectric device according to claim 1, the plurality of bumps formed on the semiconductor integrated circuit being concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. (Amended) The piezoelectric device according to claim 1, further comprising a dummy bump formed on an active element surface of the semiconductor integrated circuit.

5. (Amended) The piezoelectric device according to claim 4, the dummy bump formed on the semiconductor integrated circuit being connected to the electrode pattern on the base.

7. (Amended) The piezoelectric device according to claim 1, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. (Amended) The piezoelectric device according to claim 1, the base comprising a ceramic composite substrate.

9. (Amended) The piezoelectric device according to claim 1, each of the plurality of bumps formed on the semiconductor integrated circuit being an Au bump.

10. (Amended) The piezoelectric device according to claim 1, a protrusion being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. (Amended) The piezoelectric device according to claim 10, the protrusion being formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. (Amended) The piezoelectric device according to claim 10, the protrusion formed in the side wall of the base having a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. (Amended) The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit being set to a range between 0.05 and 0.15 mm.

14. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern of the base through the plurality of bumps.

15. (Amended) The piezoelectric device according to claim 14, the plurality of bumps formed on the semiconductor integrated circuit being formed at regular intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. (Amended) The piezoelectric device according to claim 14, further comprising a dummy bump formed on the active element surface of the semiconductor integrated circuit.

17. (Amended) The piezoelectric device according to claim 16, the dummy bump formed on the semiconductor integrated circuit being connected to the electrode pattern on the base.

19. (Amended) The piezoelectric device according to claim 14, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. (Amended) The piezoelectric device according to claim 14, the base comprising a ceramic composite substrate.

21. (Amended) The piezoelectric device according to claim 14, the plurality of bumps formed on the semiconductor integrated circuit being Au bumps.

22. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding.

23. (Amended) The piezoelectric device according to claim 22, a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit being

perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. (Amended) The piezoelectric device according to claim 22, a printing direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

25. (Amended) The piezoelectric device according to claim 22, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. (Amended) The piezoelectric device according to claim 25, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level being 80 to 90 μm in diameter and 30 to 35 μm in height, and a second level being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. (Amended) The piezoelectric device according to claim 22, the base comprising a ceramic composite substrate.

28. (Amended) The piezoelectric device according to claim 22, the plurality of bumps formed on the semiconductor integrated circuit being Au bumps.

29. (Amended) The piezoelectric device according to claim 22, a longitudinal direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

30. (Amended) The piezoelectric device according to claim 22,

a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit being different from a vibration

REMARKS

Claims 1-32 are pending. By this Amendment, the specification and claims 1-5, 7-17 and 19-30 are amended for further clarity. No new matter is added.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. 1.121(b)(iii)) and claim (37 C.F.R. 1.121(c)(ii)).

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for initial examination. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/zmc

Attachments:
Substitute Abstract
Appendix

Date: April 06, 2001

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

ABSTRACT OF THE DISCLOSURE

An opening is formed in the center of a base on which an input/output electrode pattern is formed. Meanwhile, a plurality of bumps are formed on two opposing sides of an active element surface of the semiconductor integrated circuit so as to mount the semiconductor integrated circuit in the center of the opening. The semiconductor integrated circuit is connected to the electrode pattern on the base through the plurality of bumps by ultrasonic bonding. In this way, a small and thin piezoelectric device which has superior bonding characteristics of the semiconductor integrated circuit and the base, which are subjected to flip-chip bonding, and which endures mechanical shock, thermal stress, etc., can be obtained at reduced cost.

APPENDIX

Changes to Specification:

Page 2, line 22, is deleted.

Page 2, after paragraph **[0005]**, a new heading is added.

The following are marked-up versions of the amended paragraphs:

Page 1, lines 1-4:

~~DESCRIPTION~~

PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

~~Technical Field~~1. Field of the Invention

Page 1, line 8:

~~Background Art~~2. Description of Related Art

[0008] One exemplary embodiment of the ~~The~~ present invention ~~in claim 1~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element both included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern on the base through a plurality of bumps.

[0009] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 2 is a~~ the piezoelectric device described above, ~~according to claim 1, wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on the center portion of an active element surface of the semiconductor integrated circuit.

[0010] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 3 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about the center of an active element surface of the semiconductor integrated circuit.

[0011] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 4 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0012] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 5 a~~ the piezoelectric device ~~according to claim 4~~ described above, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0013] In another exemplary embodiment of the ~~The~~ present invention, ~~in claim 6 is a~~ the piezoelectric device ~~according to claim 1,~~ described above further ~~comprising~~ includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator, the layered part ~~comprising~~ including at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0014] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 7 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

[0015] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 8 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ the base ~~comprises~~ may consist of a ceramic composite substrate.

[0016] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 9 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

[0017] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 10 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

[0018] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 11 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ the protrusion is formed in each of the side walls of the base facing the two sides along the longitudinal direction of the semiconductor integrated circuit.

[0019] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 12 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ the protrusion formed in the side wall of the base has substantially the same height as, or is higher than, the semiconductor integrated circuit.

[0020] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 13 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

[0021] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 14~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a

piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the opening, and the semiconductor integrated circuit is connected to the electrode pattern of the base through the plurality of bumps.

[0022] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 15 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals at the center portion of the active element surface of the semiconductor integrated circuit.

[0023] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 16 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0024] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 17 is a~~ the piezoelectric device ~~according to claim 16~~ described above, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0025] In another exemplary embodiment of the present ~~The~~ invention, ~~in claim 18 is a~~ the piezoelectric device ~~according to claim 14~~ described above, further includes ~~comprising~~ a layered part on which the piezoelectric resonator is mounted and which surrounds the semiconductor integrated circuit, the layered part ~~comprising~~ including at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0026] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 19 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0027] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 20 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the base ~~comprises~~ includes a ceramic composite substrate.

[0028] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 21 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0029] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 22~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern is formed, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern through the plurality of bumps by ultrasonic bonding ~~means~~.

[0030] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 23 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular

to the two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

[0031] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 24 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0032] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 25 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0033] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 26 is a~~ the piezoelectric device ~~according to claim 25~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

[0034] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 27 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the base ~~comprises~~ consists of a ceramic composite substrate.

[0035] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 28 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0036] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 29 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0037] In another exemplary embodiment of the present ~~The~~ invention, ~~in claim 30 is a~~ the piezoelectric device ~~according to claim 22, comprising~~ described above includes the semiconductor integrated circuit and the piezoelectric resonator element in included in the package, wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

[0038] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 31~~ is a method for manufacturing a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: ~~comprising:~~ a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

[0039] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 32~~ is a method for manufacturing a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method ~~comprising~~ may include: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which metallic bump is

formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step; a step of filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Page 7, line 22:

~~Brief Description of the Drawings~~

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] Figs. 1(A)-(B) are~~Fig. 1 is a~~ structural diagrams~~diagram~~ of a piezoelectric device according to the present invention;

Fig. 2 is a diagram illustrating the formation of a bump on a wafer of the piezoelectric device of the present invention;

Fig. 3 is a diagram showing the shape of the bump of the piezoelectric device of the present invention;

Fig. 4 is a diagram showing the shape of another bump of the piezoelectric device of the present invention;

Fig. 5 is a process diagram illustrating a flip-chip bonding process of the present invention;

Fig. 6 is a stress distribution map according to FEM analysis;

Fig. 7 is a structural diagram showing another embodiment of the present invention;

Fig. 8 is a structural diagram showing another embodiment of the present invention;

Fig. 9 is a structural diagram showing another embodiment of the present invention;

Figs. 10(A)-(B) are~~Fig. 10 is~~ a plan view and a front view, respectively, showing another embodiment of the present invention;

Figs. 11(A)-(B) are~~Fig. 11 is~~ a plan view and a front view, respectively, showing another embodiment of the present invention;

Fig. 12 is a structural diagram showing another embodiment of the present invention;

Fig. 13 is a structural diagram showing a cross-section of a bonded portion of the present invention;

Fig. 14 is a structural diagram showing yet another embodiment of the quartz crystal oscillator of the present invention;

Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14; and

Figs. 16(A)-(B) are~~Fig. 16 is a~~ structural diagrams~~diagram~~ of a conventional piezoelectric device.

Page 8, line 25:

~~Best Mode for Carrying Out the Invention~~

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0043] ~~Fig. 1 is a~~ Figs. 1(A)-(B) are structural ~~diagram~~ diagrams of a surface-mount type quartz crystal oscillator according to an embodiment of the present invention.

[0044] As shown in a plan view of Fig. 1(A) and in a front view of Fig. 1(B), on a first layer of a base 1 ~~comprising~~ consisting of a ceramic insulating substrate having at least three layers and a seal ring of Fe-Ni alloy or the like, stamped to a frame shape, an electrode pattern 3 for forming a connection with a semiconductor integrated circuit (IC chip: hereinafter referred to as the IC chip) 2 is metallized by means of printing by using metal wiring material such as W (tungsten), Mo (molybdenum). On the top thereof, Ni plating and Au plating, etc., are provided.

[0058] The wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal ~~collet,~~ collet, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned and is chip-mounted on a mounting area of the base 1 with high precision by a system such as an image recognition system provided in the flip-chip bonding apparatus.

[0066] As shown in ~~Fig. 1,~~ Figs. 1(A)-(B), a configuration in which an opening 16 is formed in the center of the base 1 and the IC chip 2 is mounted in the center of the opening 16 is employed. Thus, when the quartz crystal oscillator 13 is exposed to stress, by this configuration, the stress is evenly applied to the IC chip 2, preventing the stress from concentrating in a specific portion.

[0077] As shown in ~~Fig. 1,~~ Figs. 1(A)-(B), the AT-cut quartz crystal resonator 6 is connected and fixed by the conductive adhesive 9 to mounting electrodes 21 and 22 of the mounting portion 8 provided in the second layer 5 of the base 1.

[0089] Furthermore, in order for the underfill material 23 to properly permeate to the bonded portion of the bumps 4, the second layer 5 on which the AT-cut quartz crystal resonator 6 is mounted ~~comprises~~ may include two layers, i.e., ~~an a~~ a first layer 24 ~~(first layer)~~ and a ~~b~~ second layer 25 ~~(second layer)~~. The opening portion of the ~~a~~ first layer 24 is formed to be larger than the opening portion of the ~~b~~ second layer 25. By forming the second layer ~~5~~ 25 in such a manner, the underfill material 23 properly permeates to the bonded portion of the bumps 4 and a highly reliable bonding structure is obtained.

[0107] In this embodiment, the vibration direction US2 of the ultrasonic waves for ultrasonic bonding and for forming bumps on the IC chip 2 shown in Fig. 15, and vibration direction US1 of the ultrasonic waves for performing a ultrasonic bonding of the IC chip 2 and the base 1 shown in Fig. 14 are set to be different, preferably, in directions which differ from one another by 90 degrees.

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being ~~both~~ included in a package,

~~wherein an opening is formed in a center of a base provided with an input/output electrode pattern,~~ the semiconductor integrated circuit ~~is~~ being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern on the base through ~~a~~ the plurality of bumps.

2. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ further comprising a dummy bump ~~is~~ formed on an active element surface of the semiconductor integrated circuit.

5. (Amended) The piezoelectric device according to claim 4, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit ~~is~~ being connected to the electrode pattern on the base.

7. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, a first level ~~one~~ having a diameter 0.8 to 0.9 times and ~~the other~~ a second level having a diameter 0.4 to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

9. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being an Au bump.

10. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ a protrusion ~~is~~ being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. (Amended) The piezoelectric device according to claim 10, ~~wherein~~ the protrusion ~~is~~ being formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. (Amended) The piezoelectric device according to claim 10, ~~wherein~~ the protrusion formed in the side wall of the base ~~has~~ having a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. (Amended) The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit ~~is~~ being set to a range between 0.05 and 0.15 mm.

14. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

~~wherein an opening is formed in the center of a base provided with an input/output electrode pattern,~~ a plurality of bumps ~~are~~ being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit ~~is~~ being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern of the base through the plurality of bumps.

15. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being formed at regular intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ further comprising a dummy bump ~~is~~ formed on the active element surface of the semiconductor integrated circuit.

17. (Amended) The piezoelectric device according to claim 16, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit ~~is~~ being connected to the electrode pattern on the base.

19. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level having a diameter 0.8 to 0.9 times and ~~the other~~ a second level

having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

21. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being Au bumps.

22. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

~~wherein an opening is formed in the center of a base provided with an input/output electrode pattern,~~ a plurality of bumps ~~are~~ being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit ~~is~~ being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding ~~means~~.

23. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~is~~ being perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a printing direction of the electrode pattern on the base ~~and~~ being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~are the same~~.

25. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level having a diameter 0.8 to 0.9 times and ~~the other~~ a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. (Amended) The piezoelectric device according to claim 25, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level being 80 to 90 μm in diameter and 30 to 35 μm in height, and ~~the other~~ a second level being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

28. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being Au bumps.

29. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a longitudinal direction of the electrode pattern on the base ~~and~~ being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~are the same~~.

30. (Amended) The piezoelectric device according to claim 22, ~~comprising the semiconductor integrated circuit and the piezoelectric resonator element in included in the package,~~

~~wherein~~ a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit ~~and~~ being different from a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package ~~are different from each other~~.

~~Fig. 1~~

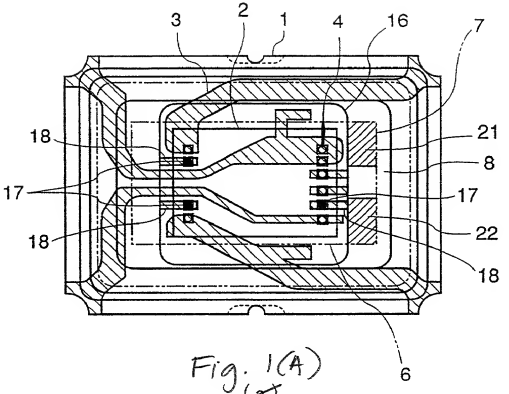
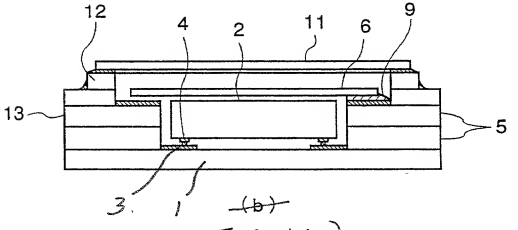


Fig. 1(A)
~~(a)~~



~~(b)~~
FIG. 1(B)

Fig. 2

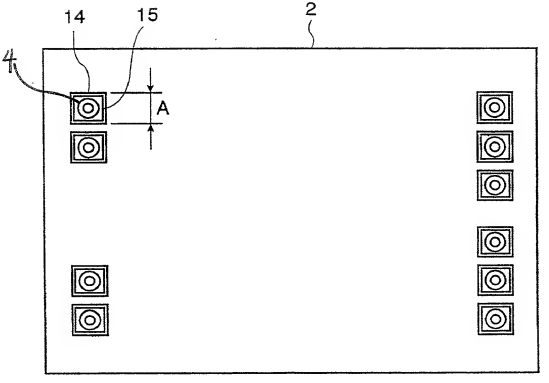


Fig. 3

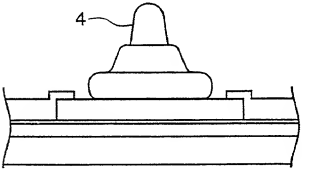


Fig. 7

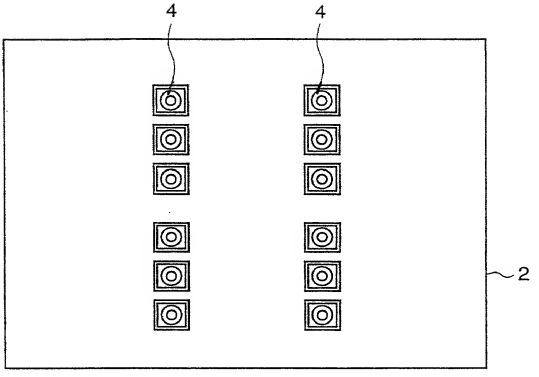


Fig.8

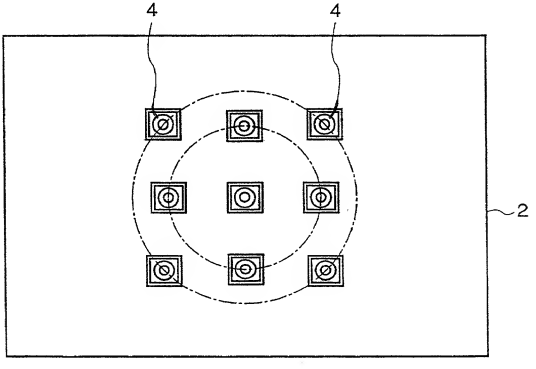
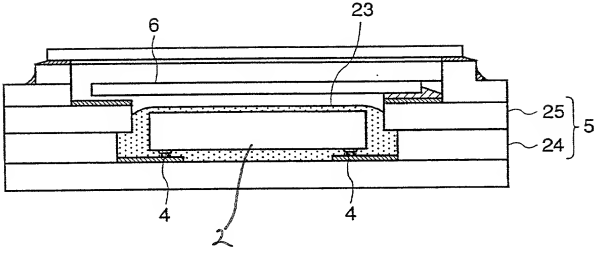
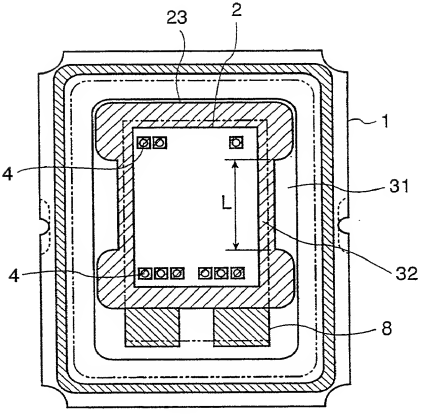


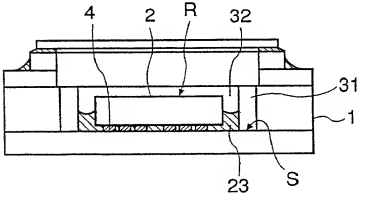
Fig. 9



~~Fig. 10~~

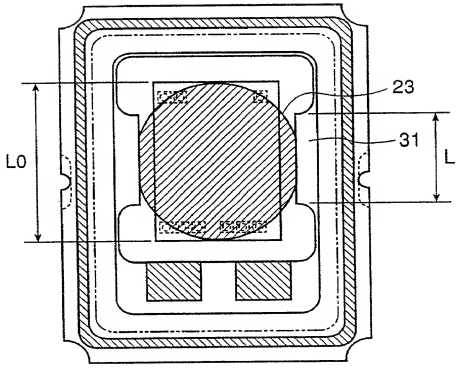


(a)
Fig. 10(A)

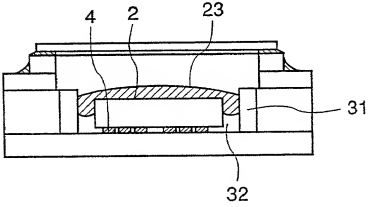


(b)
Fig. 10(B)

Fig. 11

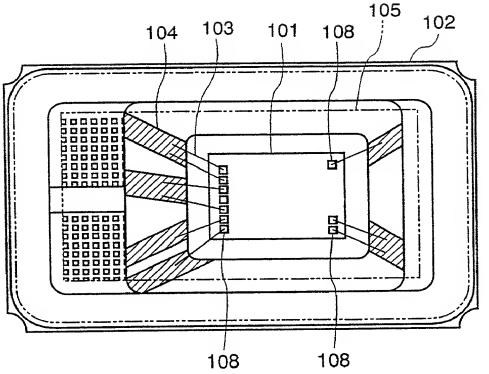


(a)
Fig. 11(A)

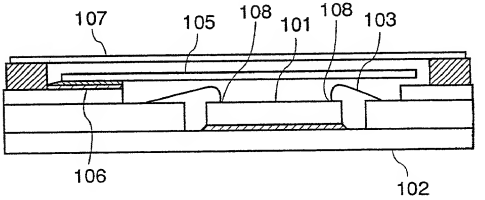


(b)
Fig. 11(B)

~~Fig. 16~~



(a) Fig. 16(A)



~~(b)~~

Fig. 16(B)

DESCRIPTION

PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

Technical Field

[0001] The present invention relates to a piezoelectric device in which a semiconductor integrated circuit and a piezoelectric resonator element are included in a package, and to a method for manufacturing the same.

Background Art

[0002] In recent years, hard disk drives (HDD), mobile computers, information apparatuses such as IC cards and portable communication apparatuses such as cellular phones, phones for automobiles have undergone dramatic miniaturization. Accordingly, piezoelectric devices such as piezoelectric oscillators, voltage-controlled oscillators (VCXO), temperature-compensated oscillators (TCXO), SAW oscillators, real time clock modules for use in these apparatuses are also required to be smaller and thinner. Also, surface-mounting type piezoelectric devices capable of being mounted on both sides of the circuit board of the device are desired.

[0003] An example of a conventional piezoelectric device will be explained using a quartz crystal oscillator shown in structural diagrams of Figs. 16(A) and 16(B), the quartz crystal oscillator using a semiconductor integrated circuit of single-chip type having an oscillating circuit and an AT-cut quartz crystal resonator as a piezoelectric resonator element.

[0004] In the conventional quartz crystal oscillator in Figs. 16(A) and 16(B), an IC chip 101 having an oscillating circuit is bonded and fixed by a conductive adhesive, etc., to the bottom face of a base 102 formed of a ceramic insulating substrate, is electrically connected by Au wire-bonding lines 103 to input/output electrodes 104 at the external periphery of the bottom face of the base 102. The input/output electrodes 104 are metallized by metal such as tungsten (W), molybdenum (Mo) and are plated in multiple layers by Ni plating and Au plating, etc. More specifically, a plurality of electrodes 108 are provided in the IC chip 101 and the

electrodes 108 are electrically connected to the above-described input/output electrodes 104, etc., by the wire-bonding lines 103.

[0005] A rectangular-shaped AT-cut quartz crystal resonator 105 is electrically connected to a mounting portion 106 of the base 102 and is fixed thereto by a conductive adhesive or the like. A plated layer at the top portion of the base 102 and a metallic lid 107 are connected by melting a metallic cladding material such as solder formed on the lid 107 at a high temperature so as to provide a hermetic seal, while maintaining an N_2 (nitrogen) atmosphere or to a vacuum atmosphere in the inner portion.

[0006] The above-described conventional quartz crystal oscillator requires an area around the IC chip 101 for wiring the Au wire-bonding lines 103, and a sufficient height in the direction of the package thickness must be secured to accommodate the loops of the Au wire-bonding lines 103. Also, a gap must be provided between the Au wire-bonding lines 103 and the AT-cut quartz crystal resonator 105. Such a configuration prevents further miniaturization of quartz crystal oscillators.

[0007] Objects of the present invention are to solve the above-described problems and to provide at reduced cost a small and thin piezoelectric device, such as a quartz crystal oscillator, which can withstand mechanical impacts and has a thickness of 1 mm or less, and to provide a method for manufacturing the piezoelectric device.

Disclosure of Invention

[0008] The invention in claim 1 is a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element both included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern on the base through a plurality of bumps.

[0009] The invention in claim 2 is a piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on the center portion of an active element surface of the semiconductor integrated circuit.

[0010] The invention in claim 3 is a piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about the center of an active element surface of the semiconductor integrated circuit.

[0011] The invention in claim 4 is a piezoelectric device according to claim 1, wherein a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0012] The invention in claim 5 a piezoelectric device according to claim 4, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0013] The invention in claim 6 is a piezoelectric device according to claim 1, further comprising a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator, the layered part comprising at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0014] The invention in claim 7 is a piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

[0015] The invention in claim 8 is a piezoelectric device according to claim 1, wherein the base comprises a ceramic composite substrate.

[0016] The invention in claim 9 is a piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

[0017] The invention in claim 10 is a piezoelectric device according to claim 1, wherein a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

[0018] The invention in claim 11 is a piezoelectric device according to claim 10, wherein the protrusion is formed in each of the side walls of the base facing the two sides along the longitudinal direction of the semiconductor integrated circuit.

[0019] The invention in claim 12 is a piezoelectric device according to claim 10, wherein the protrusion formed in the side wall of the base has substantially the same height as, or is higher than, the semiconductor integrated circuit.

[0020] The invention in claim 13 is a piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

[0021] The invention in claim 14 is a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the opening, and the semiconductor integrated circuit is connected to the electrode pattern of the base through the plurality of bumps.

[0022] The invention in claim 15 is a piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals at the center portion of the active element surface of the semiconductor integrated circuit.

[0023] The invention in claim 16 is a piezoelectric device according to claim 14, wherein a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0024] The invention in claim 17 is a piezoelectric device according to claim 16, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0025] The invention in claim 18 is a piezoelectric device according to claim 14, further comprising a layered part on which the piezoelectric resonator is mounted and which surrounds the semiconductor integrated circuit, the layered part comprising at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0026] The invention in claim 19 is a piezoelectric device according to claim 14, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0027] The invention in claim 20 is a piezoelectric device according to claim 14, wherein the base comprises a ceramic composite substrate.

[0028] The invention in claim 21 is a piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0029] The invention in claim 22 is a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern is formed, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern through the plurality of bumps by ultrasonic bonding means.

[0030] The invention in claim 23 is a piezoelectric device according to claim 22, wherein a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to the two opposing sides of the active element

surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

[0031] The invention in claim 24 is a piezoelectric device according to claim 22, wherein a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0032] The invention in claim 25 is a piezoelectric device according to claim 22, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0033] The invention in claim 26 is a piezoelectric device according to claim 25, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

[0034] The invention in claim 27 is a piezoelectric device according to claim 22, wherein the base comprises a ceramic composite substrate.

[0035] The invention in claim 28 is a piezoelectric device according to claim 22, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0036] The invention in claim 29 is a piezoelectric device according to claim 22, wherein the longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0037] The invention in claim 30 is a piezoelectric device according to claim 22, comprising the semiconductor integrated circuit and the piezoelectric resonator element in included in the package, wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit

and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

[0038] The invention in claim 31 is a method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

[0039] The invention in claim 32 is a method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step; a step of filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Brief Description of the Drawings

[0040] Fig. 1 is a structural diagram of a piezoelectric device according to the present invention;

Fig. 2 is a diagram illustrating the formation of a bump on a wafer of the piezoelectric device of the present invention;

Fig. 3 is a diagram showing the shape of the bump of the piezoelectric device of the present invention;

Fig. 4 is a diagram showing the shape of another bump of the piezoelectric device of the present invention;

Fig. 5 is a process diagram illustrating a flip-chip bonding process of the present invention;

Fig. 6 is a stress distribution map according to FEM analysis;

Fig. 7 is a structural diagram showing another embodiment of the present invention;

Fig. 8 is a structural diagram showing another embodiment of the present invention;

Fig. 9 is a structural diagram showing another embodiment of the present invention;

Fig. 10 is a plan view and a front view showing another embodiment of the present invention;

Fig. 11 is a plan view and a front view showing another embodiment of the present invention;

Fig. 12 is a structural diagram showing another embodiment of the present invention;

Fig. 13 is a structural diagram showing a cross-section of a bonded portion of the present invention;

Fig. 14 is a structural diagram showing yet another embodiment of the quartz crystal oscillator of the present invention;

Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14; and

Fig. 16 is a structural diagram of a conventional piezoelectric device.

Best Mode for Carrying Out the Invention

[0041] The preferred embodiments of the present inventions will be described below with reference to the drawings.

[0042] An embodiment of a piezoelectric device of the present invention is described with reference to the drawings, using as an example a quartz crystal

oscillator having a single-chip-type semiconductor integrated circuit having an oscillation circuit and an AT-cut quartz crystal resonator element as a piezoelectric resonator element.

(EMBODIMENT 1)

[0043] Fig. 1 is a structural diagram of a surface-mount type quartz crystal oscillator according to an embodiment of the present invention.

[0044] As shown in a plan view of Fig. 1(A) and in a front view of Fig. 1(B), on a first layer of a base 1 comprising a ceramic insulating substrate having at least three layers and a seal ring of Fe-Ni alloy or the like, stamped to a frame shape, an electrode pattern 3 for forming a connection with a semiconductor integrated circuit (IC chip: hereinafter referred to as the IC chip) 2 is metallized by means of printing by using metal wiring material such as W (tungsten), Mo (molybdenum). On the top thereof, Ni plating and Au plating, etc., are provided.

[0045] On an electrode pad of the IC chip 2, a metallic bump 4 made of Au or the like is formed and, by a flip-chip bonding method, is connected to the electrode pattern 3 formed on the base 1. Among various techniques of the flip-chip bonding method, the method employed in the present embodiment is one using ultrasonic waves to yield an Au-Au solid state bond.

[0046] A supported portion 7 of an AT-cut quartz crystal resonator 6 is connected and fixed by a conductive adhesive 9 to a mounting portion 8 provided in a second layer 5 of the base 1.

[0047] A metallic lid 11 is aligned with a seal ring 12 formed of an Fe-Ni alloy or the like die-cut into a frame shape, is fixed, and is hermetically sealed by seam welding.

[0048] Accordingly, a small and thin surface-mounted package type quartz crystal oscillator 13 is obtained.

[0049] Next, a bump forming process for forming the bump 4 made of Au or the like on the IC chip 2, and a flip-chip bonding process for connecting the IC chip 2 to the electrode pattern 3 formed on the base 1 will be described in detail.

[0050] For example, as shown in Fig. 2, on pads 14 of the wafer IC chip 2 which is 4 to 6 inches, a plurality of bumps 4 are formed by ultrasonic bump bonding using fine Au bonding lines each having a diameter of, for example, approximately 25 to 35 μm.

[0051] There are several possible shapes for the bump 4; in this embodiment, as shown in Fig. 3, the bump 4 having two levels is formed.

[0052] When a side of a pad opening 15 of the pad 14 of the IC chip 2 has a length A, the bump 4 is shaped to have two levels, one having a diameter of 0.8A to 0.9A, another having a diameter of 0.4A to 0.45A.

[0053] Described in terms of specific figures, when the length of one side of the pad opening 15 in the typical pad 14 is 100 μm, the bump 4 preferably has two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, the other being 40 to 45 μm in diameter and 30 to 35μm in height.

[0054] In order to form bumps on a number of (approximately several thousand) wafer IC chips 2, the working temperature for forming the bumps is preferably low and, in this embodiment, the bumps are worked at a temperature of approximately 180°C. The experiments and evaluations regarding jointing strength and range of eutectic show that the preferable temperature is, for example, a temperature in a range of 180°C to 230°C.

[0055] In order to improve the flatness of the tip portion of the second stage of the bump 4, the tip portion of the bump 4 may be crushed and leveled as shown in Fig. 4.

[0056] Next, a flip-chip bonding process for bonding the IC chip 2 provided with the bumps 4 of the above-described shape to the base 1 will be described in detail.

[0057] Fig. 5 is a process diagram illustrating a flip-chip bonding process.

[0058] The wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal collet, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned and is chip-mounted on a mounting area of the

base 1 with high precision by a system such as an image recognition system provided in the flip-chip bonding apparatus.

[0059] When the IC chip 2 contacts the electrode pattern 3 of the base 1 and load is detected by the flip-chip bonding apparatus, weight is applied at 100 grams per bump and, ultrasonic waves are simultaneously applied to bond Au in the bump 4 and Au in the electrode pattern 3 in a solid state. The conditions of the ultrasonic waves are determined by the power of ultrasonic waves and application period of the ultrasonic waves. In order to conduct the bonding, a proper temperature is required, and the base 1 is preheated at, for example, a temperature in a range between approximately 150°C and 200°C. The base 1 is also heated in a similar manner during the ultrasonic wave processing.

[0060] In the flip-chip bonding apparatus, a sensor for detecting a height direction of the IC chip 2 is provided and by checking and controlling the height data, the process can be carried out as if the height of the bumps 4 were uniform.

[0061] The working parameters employed in the present embodiment is to apply load of approximately 100 grams per bump and, for the parameters of the ultrasonic waves, a parameter value determined by the size of the IC chip 2 and the number of the bumps 4 is used.

[0062] Fig. 6 is a stress distribution map of the IC chip 2 and the vicinity of the bumps 4 during reflow using FEM (Finite Element Method) analysis or when thermal stress due to a cycling test, etc., is applied to the quartz crystal oscillator 13.

[0063] From this stress distribution map, it can be understood that the stress value is varied depending on the position of the bump and that significant stress concentration acts in the vicinities of the bumps 4 arranged at the corners of the IC chip 2 and in the portion with fewer bumps 4.

[0064] When the stress is applied to the vicinity of the bumps 4 as described above, a failure such as the bump 4 and the electrode pattern 3 becoming disconnected, is likely to occur. Such failure is likely to occur especially when a high temperature such as that during reflow is suddenly applied to the quartz crystal

oscillator 13. Such failure may also occur due to aging, dropping a device such as a portable device having the thin quartz crystal oscillator 13 inside, and mechanical shock such as vibrations.

[0065] The thermal stress and mechanical stress due to dropping and vibration are related to the overall structure of the base 1, and it is another object of the present invention to provide a configuration of the quartz crystal oscillator 13 in which stress is not concentrated around the bump 4. Essential points of such a configuration will be described below.

[0066] As shown in Fig. 1, a configuration in which an opening 16 is formed in the center of the base 1 and the IC chip 2 is mounted in the center of the opening 16 is employed. Thus, when the quartz crystal oscillator 13 is exposed to stress, by this configuration, the stress is evenly applied to the IC chip 2, preventing the stress from concentrating in a specific portion.

[0067] Next, a configuration in which dummy bumps 17 are formed will be explained. The dummy bumps 17 are connected to an electrode pattern 18 laid out on the base 1. In this embodiment, the electrode pattern 18 is not connected to the input/output electrodes and is configured to be electrically isolated.

[0068] By employing the structure with the dummy bumps 17 formed, the arrays of the bumps 4 at two opposing sides become even, equally sharing the stress applied to the vicinity of the bumps 4.

[0069] Consequently, in this configuration, stress is not concentrated in a specific area and well-balanced bonding characteristics resistant to thermal stress and mechanical stress can be obtained.

[0070] Next, the direction in which ultrasonic waves are applied and deformation of the bumps 4 will be described.

[0071] During the process of applying ultrasonic waves to perform solid state bonding of Au in the bump 4 and Au in the electrode pattern 3, the initial two-level shape of the bump 4 shown in Fig. 3 is deformed and connected. At this time, in order to prevent a short-circuit between the adjacent bumps 4 and in order to perform

bonding of all the bumps 4 and the electrode pattern 3 in an even manner, the way in which the bumps 4 are arrayed relative to the application direction of the ultrasonic waves, the directions in which the electrode pattern 3 is printed on the base 1, and the direction in which the ultrasonic waves are applied are regulated.

[0072] To be specific, the bonding process is carried out in such a manner that the vibration direction of ultrasonic waves applied to the IC chip 2 is substantially perpendicular to the two opposing sides of an active element surface of the IC chip 2 provided with the plurality of the bumps 4.

[0073] Fig. 13 is a sectional view showing the bonded portion of the electrode pattern 3 and the bump 4.

[0074] Because the electrode pattern 3 is formed by applying electrode material by thick-film printing, both ends thereof sag, and the bump 4 and the electrode pattern 3 are not bonded at such portions.

[0075] Accordingly, when the process is performed by adjusting the vibration direction of the ultrasonic waves to be perpendicular to the longitudinal direction of the electrode pattern 3, there is a problem in that bonding is not carried out in an even manner and that sufficient jointing force cannot be obtained. Thus, in this embodiment, the bonding process is carried out in such a manner that the vibration direction of the ultrasonic waves applied to the IC chip 2 is set to be the same as the longitudinal direction of the electrode pattern 3 on the base 1 and the printing direction of the electrode pattern 3.

[0076] Next, a process for mounting the AT-cut quartz crystal resonator 6 to the base 1 will be explained.

[0077] As shown in Fig. 1, the AT-cut quartz crystal resonator 6 is connected and fixed by the conductive adhesive 9 to mounting electrodes 21 and 22 of the mounting portion 8 provided in the second layer 5 of the base 1.

[0078] Then, the entire package including the IC chip 2 and the AT-cut quartz crystal resonator 6 are subjected to an annealing treatment at a high temperature while hardening the conductive adhesive 9. This also has the effect of

removing gasses emitted from the conductive adhesive 9, the base 1, and so forth. Generally, the treatment is carried out for 1 to 2 hours at a high temperature in a range between 200°C and 300°C.

[0079] By this thermal treatment, an Al-Au eutectic reaction in the bump 4, an Au-Au solid-state bonding reaction, stress release in the bonded portion, and so forth are promoted, and bonding characteristics such as bonding strength of the bump 4 change. In this embodiment, conditions for forming the bump 4 and conditions for the flip chip bonding are determined taking into consideration such heat history after the flip chip bonding.

[0080] Furthermore, the metallic lid 11 is aligned with the seal ring 12 of Fe-Ni alloy or the like, which is stamped into a frame shape, on the base 1, and is hermetically sealed by seam welding.

(Embodiment 2)

[0081] Fig. 7 is a plan view illustrating the structure of a quartz crystal oscillator of another embodiment of the present invention.

[0082] This quartz crystal oscillator has a structure in which a plurality of bumps 4 are formed at regular intervals on the center portion of the active element surface of the IC chip 2.

[0083] By employing this structure, the stress applied to the bumps 4 can be evenly distributed and a disconnection failure of the bump 4 and the electrode pattern 3 is eliminated. Also by employing this structure, the bonding process using ultrasonic waves is carried out in a well-balanced manner, and failure such as the IC chip 2 being mounted in a slanted manner is eliminated.

(Embodiment 3)

[0084] Fig. 8 is a plan view illustrating the structure of a quartz crystal oscillator according to yet another embodiment of the present invention.

[0085] This quartz crystal oscillator has a structure in which a plurality of bumps 4 formed on the IC chip 2 are concentrically formed about the center of the active element surface of the IC chip 2.

[0086] As in Embodiment 2, the stress applied to the bumps 4 can be evenly distributed, and a disconnection failure of the bump 4 and the electrode pattern 3 is eliminated. Also, the bonding process using ultrasonic waves is carried out in a well-balanced manner, and failure such as the IC chip 2 being mounted in a slanted manner is eliminated.

(Embodiment 4)

[0087] Fig. 9 is a structural diagram showing the structure of a quartz crystal oscillator according to still another embodiment of the present invention.

[0088] In this quartz crystal oscillator, an underfill material 23 is applied so as to cover the rear surface of the IC chip 2. This underfill material 23 not only enhances the reliability of the bonding, but also serves to radiate heat from the IC chip 2 by improving thermal conductivity.

[0089] Furthermore, in order for the underfill material 23 to properly permeate to the bonded portion of the bumps 4, the second layer 5 on which the AT-cut quartz crystal resonator 6 is mounted comprises two layers, i.e., an a layer 24 (first layer) and a b layer 25 (second layer). The opening portion of the a layer 24 is formed to be larger than the opening portion of the b layer 25. By forming the second layer 5 in such a manner, the underfill material 23 properly permeates to the bonded portion of the bumps 4 and a highly reliable bonding structure is obtained.

(Embodiment 5)

[0090] Figs. 10(A) and 10(B) are structural diagrams showing the structure of a quartz crystal oscillator according to yet another embodiment of the present invention.

[0091] As shown in Fig. 10(A), in this quartz crystal oscillator, for example, protrusions 31 are formed in the side walls of the base 1 which face the two sides along the longitudinal direction of the IC chip 2. A gap 32 between the IC chip 2 and the protrusion 31 is set to be 0.05 to 0.15 mm, for example. In this embodiment, the gap 32 is set to 0.15 mm, for example.

[0092] As in Embodiment 1, on the electrode pad of the IC chip 2, the bump 4 made of metal such as Au is formed and is connected by the flip-chip bonding process to the electrode pattern 3 formed on the base 1.

[0093] Next, the method for applying the underfill material 23 on the rear surface of the IC chip 2 so that the underfill material 23 completely fills, without gap, the portion of the IC chip 2 in which the bumps 4 are provided, as shown in Figs. 11(A) and 11(B), will be explained in detail.

[0094] The underfill material 23 applied to the IC chip 2 through an applicator such as a dispenser, only spreads over the rear surface of the IC chip 2 due to surface tension, as shown in Fig. 11(B), and is prevented from flowing to the region with the bumps 4.

[0095] Then, as shown in Fig. 11(A), the protrusions 31 are formed on the side walls of the base 1 facing the two sides along the longitudinal direction of the IC chip 2. Because of these, the underfill material 23 applied through the applicator such as the dispenser contacts the protrusions 31 at the peripheral portion thereof, and spreads. The underfill material 23 permeates the gap 32 between the IC chip 2 and the protrusions 31, and completely fills the portion of the IC chip 2 provided with the bumps 4, without gaps.

[0096] Here, a width L of the protrusions 31 is set to 1/3 to 1/2 of the width L0 of the IC chip 2. By so setting the dimension of the width of the protrusion 31, the underfill material 23 is prevented from overflowing the mounting portion 8, etc. It also serves to urge the underfill material 23 to spread to the region of the IC chip 2 provided with the bump 4.

[0097] As shown in Fig. 10(B), the protrusions 31 are formed to be higher than the rear surface R of the IC chip 2 and are formed down to the bonding surface S of the base 1 to which the bumps 4 are connected. By thus forming the protrusions 31, the underfill material 23 is prevented from spreading upward along the side wall of the base 1 and from spreading toward the mounting portion 8 of the AT-cut quartz

crystal resonator 6. Formation of the protrusions 31 also serves to urge the underfill material 23 to spread to the bonding surface of the base 1.

[0098] The gap 32 only needs to be wider than the particles of the underfill material 23, and, ideally, 0.05 mm is optimum from various permeation characteristic experiments concerning the underfill material 23.

[0099] The protrusion 31 may be shaped to have recesses 33, as shown in Fig. 12.

[0100] Consequently, as shown in Fig. 10(B), the underfill material 23 completely fills the gap provided at the portion of the IC chip 2 having the bumps 4, and covers the vicinity of the bumps 4.

[0101] The underfill material 23 not only enhances the reliability of the bonding, but also serves to radiate the heat from the IC chip 2 by improving thermal conductivity.

[0102] As in the above, by using highly reliable and inexpensive components such as ceramic and metal, a thin and small, for example, 2 to 3.2 mm in length, 2 to 2.5 mm in width, and 0.7 to 1.0 mm in thickness, piezoelectric oscillator of high reliability can be provided at reduced cost.

(Embodiment 6)

[0103] Fig. 14 is a structural diagram illustrating the structure of a quartz crystal oscillator according to yet another embodiment of the present invention; and Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14.

[0104] During the process for forming the bumps, as shown in Fig. 2, the plurality of bumps 4 are formed on the pads 14 of the wafer IC chip 2 which is, for example, 4 to 6 inches by ultrasonic bump bonding using fine Au bonding lines each having a diameter of, for example, approximately 25 to 35 μm.

[0105] During the flip chip bonding process (FCB process), as shown in the process diagram of the flip-chip bonding process in Fig. 5, the wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal collet or the like, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned

and is chip-mounted on a mounting area of the base 1 with high precision by a system such as an image recognition system provided in the flip chip bonding apparatus.

[0106] Since the pad 14 provided with the bump 4 is, as in above, loaded several times with weight and ultrasonic waves, it is possible that the pad 14 suffers from damage. However, this embodiment prevents such damage in a manner described below.

[0107] In this embodiment, the vibration direction US2 of the ultrasonic waves for ultrasonic bonding and for forming bumps on the IC chip 2 shown in Fig. 15, and vibration direction US1 of the ultrasonic waves for performing a ultrasonic bonding of the IC chip 2 and the base 1 are set to be different, preferably, in directions which differ from one another by 90 degrees.

[0108] By setting the vibration direction US1 and the vibration direction US2 differently, damage to the pad 14 due to repetitively applying a load by ultrasonic waves can be prevented.

[0109] The present invention is not limited to the above-described embodiments, and various modifications are possible without departing from the scope of the claims.

[0110] For example, although the description has been made with regard to a quartz crystal oscillator in which a single-chip-type semiconductor integrated circuit having an oscillating circuit is used and in which an AT-cut quartz crystal resonator element is used as a piezoelectric resonator element, the present invention is not limited to this. For example, the present invention can be applied to any piezoelectric device having a semiconductor integrated circuit such as a voltage-controlled oscillator (VCXO), a temperature-compensated oscillator (TCXO), a SAW oscillator, real time clock modules. Furthermore, the present invention is also applicable to a piezoelectric device in which a quartz crystal resonator chip or a SAW chip is mounted in a package by flip-chip bonding.

[0111] As described above, according to the present invention, because of the structure in which an opening is formed in the center of the base provided with an

input/output electrode pattern, a semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected by a plurality of bumps to the electrode pattern on the base, the stress is evenly distributed over the semiconductor integrated circuit and stress concentration at a specific bump can be eliminated. Accordingly, a piezoelectric oscillator of superior configuration which is free of jointing failure between the bump and the electrode pattern can be provided.

[0112] According to the present invention, because of the structure in which dummy bumps are formed on the active element surface of the semiconductor integrated circuit, and the dummy bumps of the semiconductor integrated circuit are connected to the electrode pattern on the base, the stress applied to the bumps can be evenly distributed. Also, a bonding process using ultrasonic waves can be carried out in a well-balanced manner, the semiconductor integrated circuit is prevented from being mounted in an angled manner, and a piezoelectric oscillator of high quality can be provided.

[0113] Furthermore, according to the present invention, by filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit, i.e., including the rear surface of the semiconductor integrated circuit, is not only the reliability of bonding between the semiconductor integrated circuit and the base enhanced, but also heat from the semiconductor integrated circuit can be conducted through the underfill material and can be radiated to the outside of the package.

[0114] According to the present invention, by regulating the vibration direction of ultrasonic waves applied to the semiconductor integrated circuit, short-circuits between adjacent bumps can be prevented, ultrasonic bonding can be carried out securely, i.e., bonding between every bump and electrode pattern can be performed in an even manner, and a high quality piezoelectric oscillator with a superior yield can be provided.

[0115] According to the present invention, by shaping each of a plurality of bumps on the semiconductor integrated circuit to have two levels, for example, one formed to be 80 to 90 μm in diameter and 30 to 35 μm in height, and the other formed to be 40 to 45 μm in diameter and 30 to 35 μm in height, the gap between the semiconductor integrated circuit and the base can be maintained to be several tens of μm (approximately 30 μm), thereby performing ultrasonic bonding in a stable manner, i.e., without experiencing short circuits, bonding shear, or the like.

[0116] According to the present invention, because a protrusion is formed in at least one side wall of the base opposing a side of the semiconductor integrated circuit, the underfill material applied through an applicator such as a dispenser can completely fill the gap which is a region of the semiconductor integrated circuit around the bumps, and the bump portion can be securely coated with the underfill material. Also, by this structure, it becomes possible to apply a little underfill material, thereby preventing the underfill material from contacting to an AT-cut quartz crystal resonator, etc., and avoiding inconveniences such as oscillation termination, and variation in oscillation frequency.

[0117] According to the present invention, by setting the vibration direction of ultrasonic waves for ultrasonic bonding and for forming the bumps on the semiconductor integrated circuit and the vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit and a package differently, damage due to repetitively applying a load by the ultrasonic waves can be prevented.

Industrial Applicability

[0118] As described above, the present invention is suitable when used as a piezoelectric device having a package including a semiconductor integrated circuit and a piezoelectric resonator element and as a method for manufacturing the same.

CLAIMS

1. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element both included in a package,

wherein an opening is formed in a center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in a center of an opening, and the semiconductor integrated circuit is connected to an electrode pattern on the base through a plurality of bumps.

2. The piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. The piezoelectric device according to claim 1, wherein the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. The piezoelectric device according to claim 1, wherein a dummy bump is formed on an active element surface of the semiconductor integrated circuit.

5. The piezoelectric device according to claim 4, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

6. The piezoelectric device according to claim 1, further comprising a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator element, the layered part comprising at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

7. The piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4

to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. The piezoelectric device according to claim 1, wherein the base comprises a ceramic composite substrate.

9. The piezoelectric device according to claim 1, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

10. The piezoelectric device according to claim 1, wherein a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. The piezoelectric device according to claim 10, wherein the protrusion is formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. The piezoelectric device according to claim 10, wherein the protrusion formed in the side wall of the base has a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

14. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element included in a package,

wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in an opening, and the semiconductor integrated circuit is connected to an electrode pattern of the base through the plurality of bumps.

15. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are formed at regular

intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. The piezoelectric device according to claim 14, wherein a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

17. The piezoelectric device according to claim 16, wherein the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

18. The piezoelectric device according to claim 14, further comprising a layered part on which the piezoelectric resonator element is mounted and which surrounds the semiconductor integrated circuit, the layered part comprising at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

19. The piezoelectric device according to claim 14, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. The piezoelectric device according to claim 14, wherein the base comprises a ceramic composite substrate.

21. The piezoelectric device according to claim 14, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

22. A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element included in a package,

wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in a center of an opening, and the

semiconductor integrated circuit is connected to an electrode pattern through the plurality of bumps by ultrasonic bonding means.

23. The piezoelectric device according to claim 22, wherein a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. The piezoelectric device according to claim 22, wherein a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

25. The piezoelectric device according to claim 22, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. The piezoelectric device according to claim 25, wherein each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. The piezoelectric device according to claim 22, wherein the base comprises a ceramic composite substrate.

28. The piezoelectric device according to claim 22, wherein the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

29. The piezoelectric device according to claim 22, wherein a longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

30. The piezoelectric device according to claim 22, comprising the semiconductor integrated circuit and the piezoelectric resonator element in included in the package,

wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

31. A method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising:

a step of forming a metallic bump on the semiconductor integrated circuit;

a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to a base by ultrasonic bonding;

a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding;

a step of mounting the piezoelectric resonator element; and

a step of hermetically sealing a metallic lid to the base.

32. A method for manufacturing a piezoelectric device comprising a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method comprising:

a step of forming a metallic bump on the semiconductor integrated circuit;

a step of connecting the semiconductor integrated circuit on which metallic bump is formed to a base by ultrasonic bonding;

a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step;

a step of filling an underfill material around the semiconductor integrated circuit so as to cover an entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit;

a step of mounting the piezoelectric resonator element; and

a step of hermetically sealing a metallic lid to the base.

ABSTRACT

An opening is formed in the center of a base 1 on which an input/output electrode pattern 3 is formed. Meanwhile, a plurality of bumps 4 are formed on two opposing sides of an active element surface of the semiconductor integrated circuit 2 so as to mount the semiconductor integrated circuit 2 in the center of the opening. The semiconductor integrated circuit 2 is connected to the electrode pattern 3 on the base 1 through the plurality of bumps 4 by ultrasonic bonding means. In this way, a small and thin piezoelectric device which has superior bonding characteristics of the semiconductor integrated circuit and the base, which are subjected to flip-chip bonding, and which endures mechanical shock, thermal stress, etc., can be obtained at reduced cost. A method for manufacturing the same is also provided.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masayuki KIKUSHIMA

Application No.: U.S. National Stage of PCT/JP99/06091

Filed: April 6, 2001 Docket No.: 108574

For: PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

REQUEST FOR APPROVAL OF DRAWING CORRECTIONS

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

The Examiner is requested to review and approve the proposed corrections to Figures 1(A)-2, 7-11(B) and 16(A)-16(B), marked in red on the attached copies of such drawing figures.

Upon approval by the Examiner, and upon allowance of this application, the formal drawings will be corrected.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Eric D. Morehouse
Registration No. 38,565

JAO:EDM/zmc

Date: April 06, 2001

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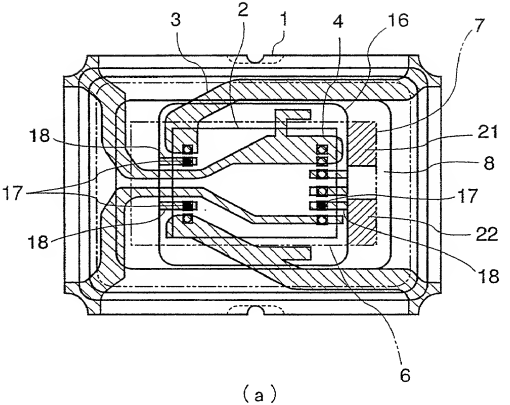
Fig. 1



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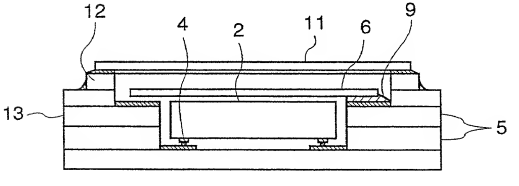

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Fig. 2

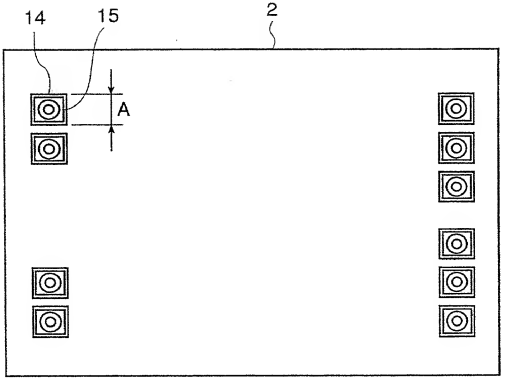


Fig. 3

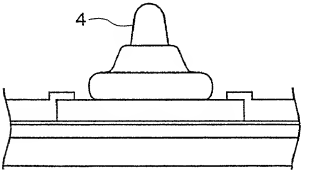


Fig. 4

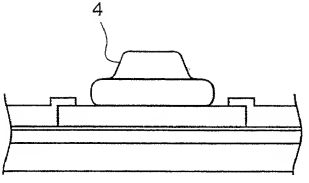


Fig. 5

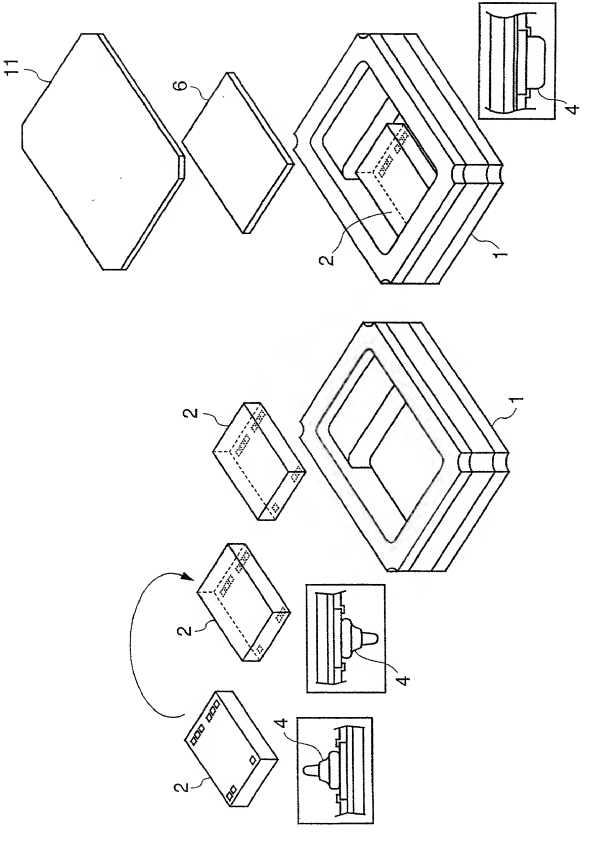
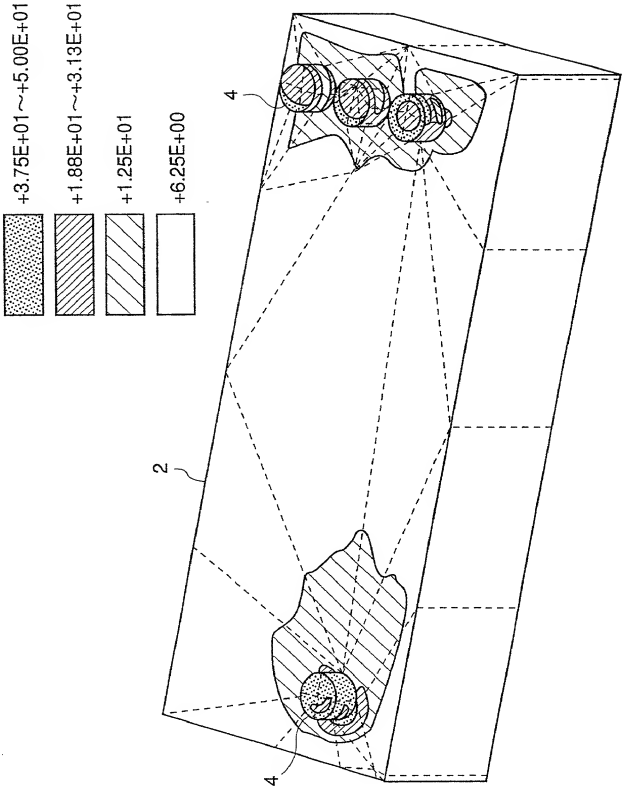


Fig. 6



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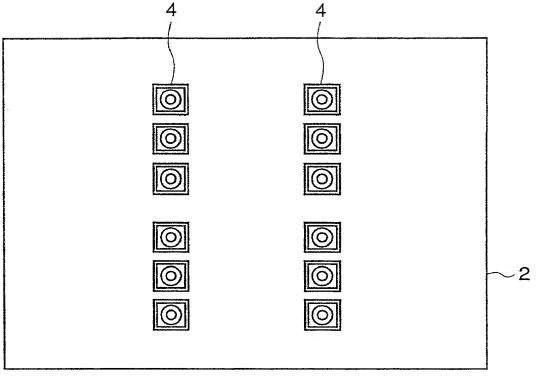


Fig.8

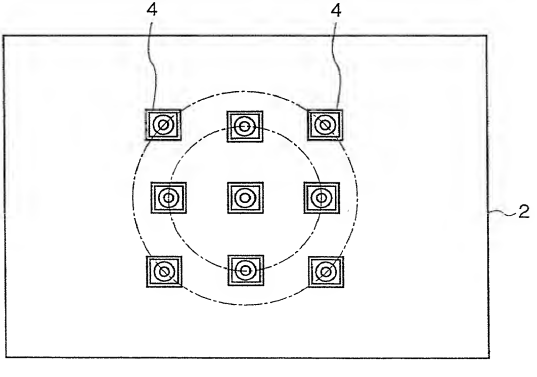


Fig. 9

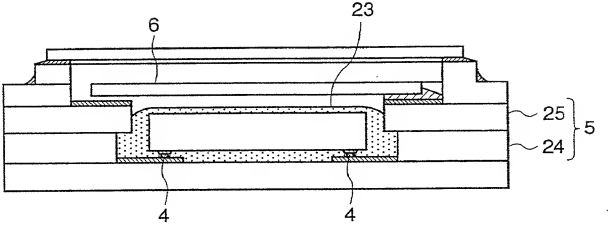
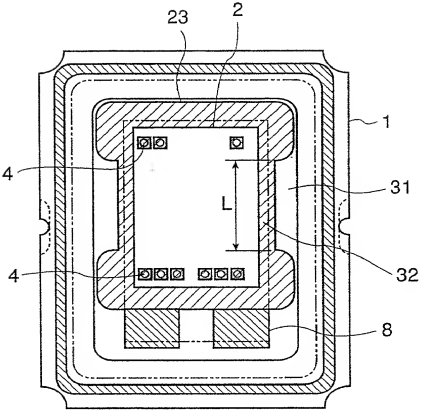


Fig. 10



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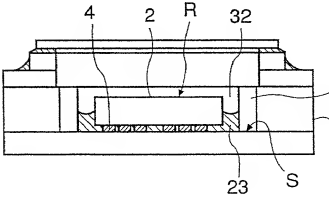
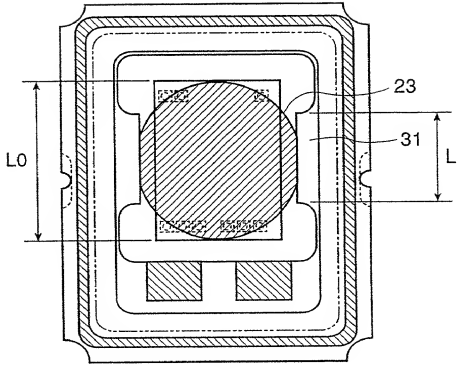


(b)

Fig. 11



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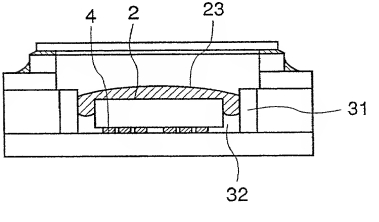

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Fig. 12

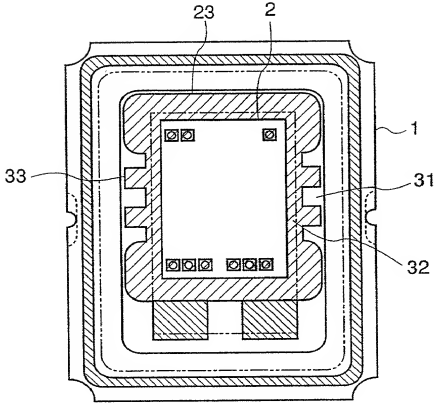


Fig. 13

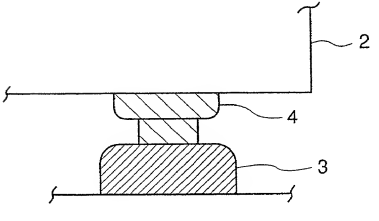


Fig. 14

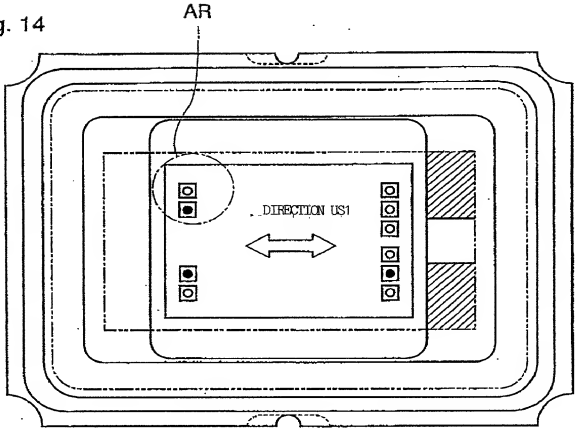


Fig. 15

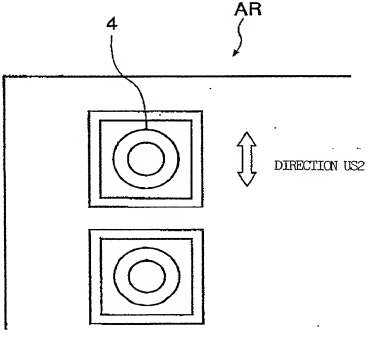
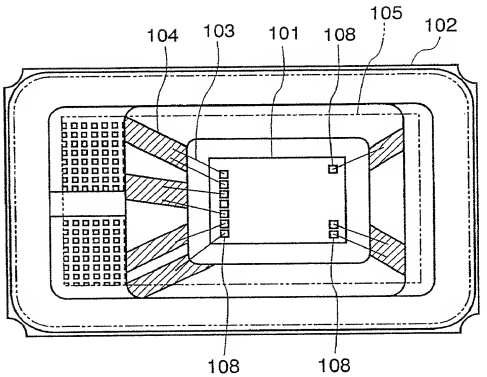


Fig. 16



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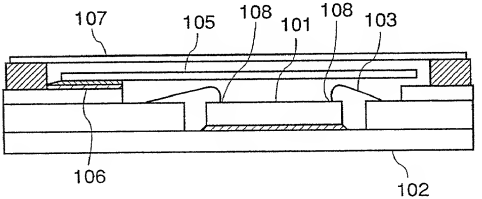

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Seiko Epson Ref. No.: F004663US00 Attorney's Ref. No.: 108574

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

圧電デバイス及びその製造方法

PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

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☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
10-343087 (Number) (番号)	Japan (Country) (国名)	02/12/1998 (Day/Month/Year Filed) (出願年月日)	☐
11-020151 (Number) (番号)	Japan (Country) (国名)	28/01/1999 (Day/Month/Year Filed) (出願年月日)	☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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PCT/JP99/06091 (Application No.) (出願番号)	November 01, 1999 (Filing Date) (出願日)	Pending (Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James A. Oliff, (Reg. 27,075)
William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

書類送付先： OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320	Send Correspondence to: OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320
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唯一または第一発明者名 菊島 正幸	Full name of sole or first inventor Masayuki KIKUSHIMA
発明者の署名 菊島正幸 日付 Mar 28, 2001	Inventor's signature Masayuki Kikushima Date Mar 28, 2001
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（第三以降の共同発明者についても同様に記載し、署名をすること）	(Supply similar information and signature for third and subsequent joint inventors.)